	TET ESTEL AS ESTONIA	**June 2013**

Series
T553-630

Phase Control Press-Pack Thyristor Type T553-630

Distributed amplifying gate
Designed for traction and industrial applications

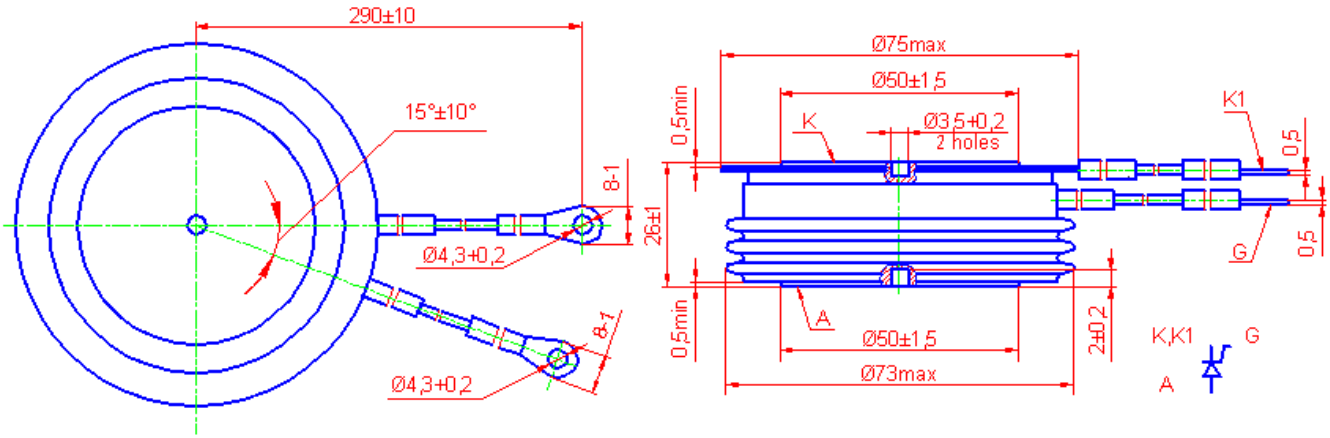
Maximum mean on-state current				I_{TAV}	**630 A**	
Maximum repetitive peak off-state and reverse voltage				U_{DRM} U_{RRM}	**3400 ÷4400 V**	
Turn-off time				**tq**	**320; 400; 500 µs**	
U_{DRM}, U_{RRM}, V	3400	3600	3800	4000	4200	4400
Voltage code	34	36	38	40	42	44
Tvj, °C	- 60 ÷ 125					

MAXIMUM ALLOWABLE RATINGS					
Symbols and parameters		Units	T553-630	Conditions	
I_{TAV}	Mean on-state current	A	630 1120	Tc=94 °C, Tc=55 °C, 180° half-sine wave, 50 Hz	
I_{TRMS}	RMS on-state current	A	989	Tc=94 °C	
I_{TSM}	Surge on-state current	kA	14 15,4	Tvj=125°C Tvj=25°C	tp=10 ms U_R=0
I^2t	Limiting load integral	kA^2s	980 1185	Tvj=125°C Tvj=25°C	
U_{DRM},U_{RRM}	Repetitive peak off-state and reverse voltage	V	3400÷4400	Tj min≤Tvj≤Tjм 180° half-sine wave, 50 Hz Gate open	
U_{DSM},U_{RSM}	Non-repetitive peak off-state and reverse voltage	V	3500÷4500	Tj min≤Tvj≤Tjм 180° half-sine wave tp=10 ms, Single pulse Gate open	
(di$_T$/dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/µs	 630 320	Tvj=125°C ; U_D=0,67 U_{DRM}, Gate pulse : 10V,5 Ω, 1µs rise time, 10 µs	
U_{RGM}	Peak reverse gate voltage	V	5	Tj min≤Tvj≤Tjм	
Tstg	Storage temperature	°C	-60÷80		
Tvj	Junction temperature	°C	-60÷125		
CHARACTERISTICS					
U_{TM}	Peak on-state voltage	V	2,3	Tvj=25°C, I_{TM}=3,14 I_{TAV}	
$U_{T(TO)}$	Threshold voltage	V	1,4	Tvj=125°C 1,57 I_{TAV}< I_T <4,71 I_{TAV}	
R_T	On-state slope resistance	mΩ	0,57		
I_{DRM} I_{RRM}	Repetitive peak off-state and reverse current	mA	 100 100	Tvj=125°C, U_D = U_{DRM} U_R= U_{RRM}	

CHARACTERISTICS				
Symbols and parameters		Units	T553-630	Conditions
I_L	Latching current	A	6	Tvj=25°C,U_D=12V Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs
I_H	Holding current	A	1,0	Tvj=25°C,U_D=12V, Gate open
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	Tvj=25°C, Tvj=-60°C U_D=12V
I_{GT}	Gate trigger direct current	A	0,3 0,85	Tvj=25°C, Tvj=-60°C
U_{GD}	Gate non-trigger direct voltage	V	0,25	Tvj=125°C, U_D = 0,67 U_{DRM}
I_{GD}	Gate non-trigger direct current	mA	10	Direct gate current
tgd	Delay time	µs	4,0	Tvj=25°C,U_D=500V I_{TM} = 630 A Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs
tgt	Turn-on time	µs	12	
tq	Turn-off time	µs	320÷500	Tvj=125°C, I_{TM}=630 A di_R/dt =10 A/µs, U_R=100V U_D = 0,67 U_{DRM} du_D/dt=50 V/µs
Qrr	Recovered charge	µC	2500	Tvj=125°C, I_{TM}=630 A di_R/dt=10 A/µs, U_R=100V
trr	Reverse recovery time	µs	36	
Irrm	Peak reverse recovery current	A	139	
$(du_D/dt)crit$	Critical rate of rise of off-state voltage	V/µs	500 1000	Tvj=125°C, U_D = 0,67 U_{DRM} Gate open
Rthjc	Thermal resistance junction to case	°C/W	0,021	Direct current, double side cooled

ORDERING							
	T	**553**	**630**	**40**	**7**	**H2**	
	1	**2**	**3**	**4**	**5**	**6**	

1. Phase control thyristor.
2. Design version.
3. Mean on-state current, A.
4. Voltage code (40=4000 V).
5. Critical rate of rise of off-state voltage (6 ≥ 500 V/µs, 7 ≥ 1000 V/µs).
6. Group of turn-off time (du_D/dt=50 V/µs, 1 ≤ 500 µs, H2 ≤ 400 µs, K2 ≤ 320 µs).



Mounting force : 19 ÷ 28 kN
Weight : 580 grams