



TET ESTEL AS
ESTONIA

June
2013

Series
T353-800TP

Phase Control Press-Pack
Thyristor
Type T353-800 TP

Center amplifying gate
Low on-state and switching losses
Designed for Railway transport

Maximum mean on-state current	I_{TAV}	800 A	
Maximum repetitive peak off-state and reverse voltage	U_{DRM} U_{RRM}	3200 ÷ 3600 V	
Turn-off time	t_q	350 μs	
U_{DRM}, U_{RRM}, V	3200	3400	3600
Voltage code	32	34	36
$T_{vj}, ^\circ C$	- 60 ÷ 125		

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	T353-800TP	Conditions
I_{TAV}	Mean on-state current	A	800 1335	$T_c=88^\circ C$, $T_c=55^\circ C$, 180° half-sine wave, 50 Hz
I_{TRMS}	RMS on-state current	A	1255	$T_c=88^\circ C$
I_{TSM}	Surge on-state current	kA	17 19	$T_{vj}=125^\circ C$ $T_{vj}=25^\circ C$ tp=10 ms $U_R=0$
I^2t	Limiting load integral	kA^2s	1445 1805	$T_{vj}=125^\circ C$ $T_{vj}=25^\circ C$
U_{DRM}, U_{RRM}	Repetitive peak off-state and reverse voltage	V	3200÷3600	$T_j \min \leq T_{vj} \leq T_{jm}$ 180° half-sine wave, 50 Hz Gate open
U_{DSM}, U_{RSM}	Non-repetitive peak off-state and reverse voltage	V	3300÷3700	$T_j \min \leq T_{vj} \leq T_{jm}$ 180° half-sine wave tp=10 ms, Single pulse Gate open
(diT/dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/ μ s	400 200	$T_{vj}=125^\circ C$; $U_D=0,67 U_{DRM}$, Gate pulse : 10V,5 Ω , 1 μ s rise time, 10 μ s
U_{RGM}	Peak reverse gate voltage	V	5	$T_j \min \leq T_{vj} \leq T_{jm}$
T_{stg}	Storage temperature	$^\circ C$	-60÷80	
T_{vj}	Junction temperature	$^\circ C$	-60÷125	

CHARACTERISTICS

U_{TM}	Peak on-state voltage	V	2,05	$T_{vj}=25^\circ C$, $I_{TM}=3,14 I_{TAV}$
$U_{T(To)}$	Threshold voltage	V	1,3	$T_{vj}=125^\circ C$
R_T	On-state slope resistance	m Ω	0,4	1,57 $I_{TAV} < I_T < 4,71 I_{TAV}$
I_{DRM} I_{RRM}	Repetitive peak off-state and reverse current	mA	100 100	$T_{vj}=125^\circ C$, $U_D = U_{DRM}$ $U_R = U_{RRM}$

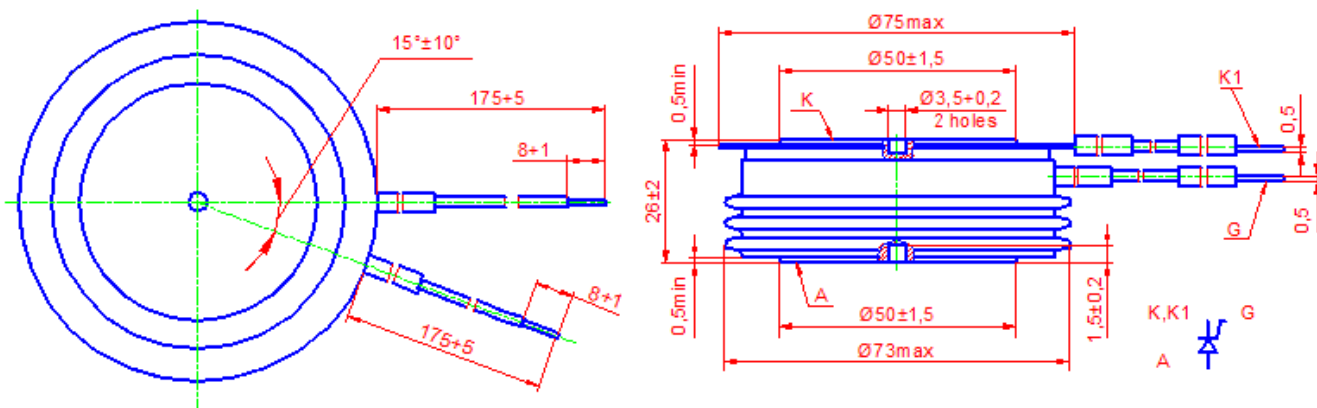
CHARACTERISTICS

Symbols and parameters		Units	T353-800TP	Conditions
I_L	Latching current	A	1,5	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$ Gate pulse : 10V, 5 μs , 1 μs rise time, 10 μs
I_H	Holding current	A	0,5	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$, Gate open
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	$U_D=12\text{V}$
I_{GT}	Gate trigger direct current	A	0,07-0,25 0,8	
U_{GD}	Gate non-trigger direct voltage	V	0,25	$T_{vj}=125^{\circ}\text{C}, U_D = 0,67 U_{DRM}$
I_{GD}	Gate non-trigger direct current	mA	10	Direct gate current
t_{gd}	Delay time	μs	3,2	$T_{vj}=25^{\circ}\text{C}, U_D=500\text{V}$ $I_{TM} = 800\text{ A}$
t_{gt}	Turn-on time	μs	10	Gate pulse : 10V, 5 μs , 1 μs rise time, 10 μs
t_q	Turn-off time	μs	350	$T_{vj}=125^{\circ}\text{C}, I_{TM}=800\text{ A}$ $di_R/dt = 10\text{ A}/\mu\text{s}, U_R=100\text{V}$ $U_D = 0,67 U_{DRM}$ $du_D/dt=50\text{ V}/\mu\text{s}$
Q_{rr}	Recovered charge	μC	2100	$T_{vj}=125^{\circ}\text{C}, I_{TM}=500\text{ A}$ $di_R/dt = 15\text{ A}/\mu\text{s}, U_R=100\text{V}$
t_{rr}	Reverse recovery time	μs	28	
I_{rrm}	Peak reverse recovery current	A	150	
$(du_D/dt)_{crit}$	Critical rate of rise of off-state voltage	$\text{V}/\mu\text{s}$	500 1000	$T_{vj}=125^{\circ}\text{C}, U_D = 0,67 U_{DRM}$ Gate open
R_{thjc}	Thermal resistance junction to case	$^{\circ}\text{C}/\text{W}$	0,02	Direct current, double side cooled

ORDERING

	T	353	800	32	7	H2	TP
	1	2	3	4	5	6	7

- Phase control thyristor.
- Design version.
- Mean on-state current, A.
- Voltage code (32=3200 V).
- Critical rate of rise of off-state voltage ($6 \geq 500\text{ V}/\mu\text{s}$, $7 \geq 1000\text{ V}/\mu\text{s}$).
- Group of turn-off time ($du_D/dt=50\text{ V}/\mu\text{s}$, $H2 \leq 400\mu\text{s}$; $K2 \leq 320\mu\text{s}$).
- Transport design.



Mounting force : 19 ÷ 28 kN
Weight : 580 grams