



TET ESTEL AS
ESTONIA

**June
2013**

**Series
T273-2500**

**Phase Control Press-Pack
Thyristor
Type T273-2500**

Center amplifying gate
Low on-state and switching losses
Designed for traction and industrial applications

Maximum mean on-state current	I_{TAV}	2500 A
Maximum repetitive peak off-state and reverse voltage	U_{DRM}	1200 ÷ 1800 V
Turn-off time	t_q	200; 250; 320 µs
U _{DRM} , U _{RRM} , V	1200	1300
Voltage code	12	13
Tvj, °C	- 60 ÷ 125	

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	T273-2500	Conditions
I _{TAV}	Mean on-state current	A	2500 3940	Tc=88 °C, Tc=55 °C, 180° half-sine wave, 50 Hz
I _{TRMS}	RMS on-state current	A	3925	Tc=88 °C
I _{TSM}	Surge on-state current	kA	50 55	Tvj=125°C Tvj=25°C
I ² t	Limiting load integral	kA ² s	12500 15125	Tvj=125°C Tvj=25°C
U _{DRM} , U _{RRM}	Repetitive peak off-state and reverse voltage	V	1200÷1800	Tj min≤Tvj≤Tjm 180° half-sine wave, 50 Hz Gate open
U _{DSM} , U _{RSM}	Non-repetitive peak off-state and reverse voltage	V	1300÷1900	Tj min≤Tvj≤Tjm 180° half-sine wave tp=10 ms, Single pulse Gate open
(di _t /dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/µs	400 200	Tvj=125°C ; Ud=0,67 U _{DRM} , Gate pulse : 10V, 5 Ω, 1µs rise time, 10 µs
U _{RGm}	Peak reverse gate voltage	V	5	Tj min≤Tvj≤Tjm
T _{stg}	Storage temperature	°C	-60÷80	
Tvj	Junction temperature	°C	-60÷125	

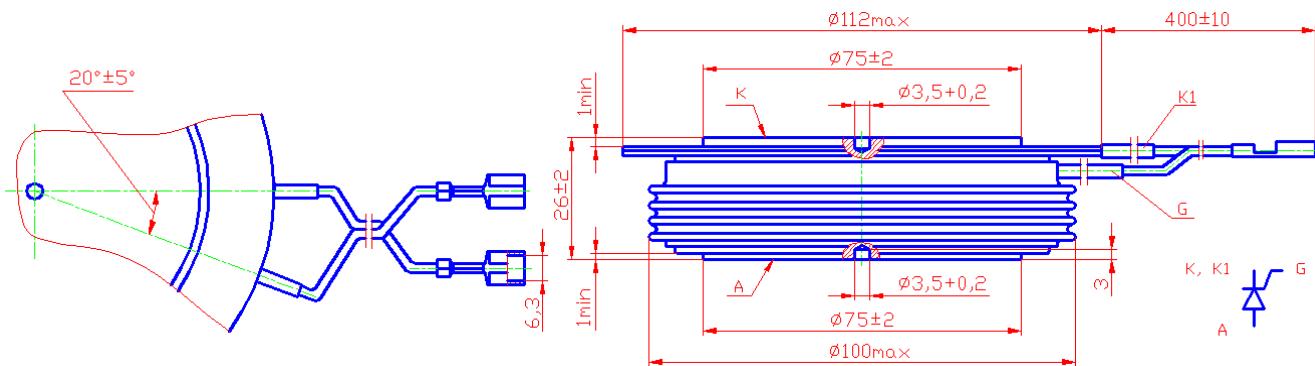
CHARACTERISTICS

U _{TM}	Peak on-state voltage	V	1,55	Tvj=25°C, I _{TM} =3,14 I _{TAV}
U _{T(TO)}	Threshold voltage	V	0,88	Tvj=125°C
R _T	On-state slope resistance	mΩ	0,092	1,57 I _{TAV} < I _T <4,71 I _{TAV}
I _{DRM} I _{RRM}	Repetitive peak off-state and reverse current	mA	150 150	Tvj=125°C, UD = U _{DRM} UR = U _{RRM}

CHARACTERISTICS				
Symbols and parameters		Units	T273-2500	Conditions
I _L	Latching current	A	3,0	Tvj=25°C, UD=12V Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs
I _H	Holding current	A	0,3	Tvj=25°C, UD=12V, Gate open
U _{GT}	Gate trigger direct voltage	V	2,5 5,0	Tvj=25°C, Tvj=-60°C UD=12V
I _{GT}	Gate trigger direct current	A	0,3 0,85	Tvj=25°C, Tvj=-60°C
U _{GD}	Gate non-trigger direct voltage	V	0,35	Tvj=125°C, UD = 0,67 U _{DRM} Direct gate current
I _{GD}	Gate non-trigger direct current	mA	20	
t _{gd}	Delay time	µs	3,2	Tvj=25°C, UD=500V ITM = 2500 A
t _{gt}	Turn-on time	µs	16	Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs
t _q	Turn-off time	µs	200÷320	Tvj=125°C, ITM=2500 A di _R /dt=10 A/µs, UR=100V UD = 0,67 U _{DRM} du _D /dt=50 V/µs
Q _{rr}	Recovered charge	µC	4500	Tvj=125°C, ITM=2500 A dir/dt=10 A/µs, UR=100V
t _{rr}	Reverse recovery time	µs	35	
I _{RRM}	Peak reverse recovery current	A	257	
(dud/dt)crit	Critical rate of rise of off-state voltage	V/µs	500 1000	
R _{thjc}	Thermal resistance junction to case	°C/W	0,01	Direct current, double side cooled

ORDERING						
T	273	2500	18	7	2	
1	2	3	4	5	6	

1. Phase control thyristor.
2. Design version.
3. Mean on-state current, A.
4. Voltage code (18=1800 V).
5. Critical rate of rise of off-state voltage ($6 \geq 500 \text{ V/}\mu\text{s}$, $7 \geq 1000 \text{ V/}\mu\text{s}$).
6. Group of turn-off time ($\text{du}_D/\text{dt}=50 \text{ V/}\mu\text{s}$, $K2 \leq 320 \mu\text{s}$; $2 \leq 250 \mu\text{s}$; $P2 \leq 200 \mu\text{s}$).



Mounting force : 36 ÷ 46 kN
Weight : 1200 grams